In the Specification:

Please amend Paragraph [0030] as follows:

Referring now to FIG. 4C and according to one embodiment of the present invention, the active TJ's 34a, 34b, 34c, 34d, 34e and 34f as well as the dummy fill silicon oxide structures 64a and 64b and the supporting metallization and silicon oxide are covered by a dielectric layer 66 that is resistant to copper diffusion. As is well known, a silicon nitride (Si_3N_4) layer having thickness of about 150 mm is particularly suitable for this purpose. Other suitable dielectric materials include Silicon oxy Nitride (SiON), Silicon Carbide (SiC) and Aluminum Oxide (Al_2O_3). The layer 66 of silicon nitride or other dielectric is then also Chemical Mechanical Polished to the top surface of the TJ structures 34a through 34f and the dummy structures 64a, 64b, and 64c ~~and 64d~~ as shown in FIG. 4D. The polished layer of silicon nitride or other dielectric material used to prevent diffusion of the copper is then covered by another dielectric layer 48 such as silicon oxide to a deposition of about 400 nm in the same manner as was discussed above with respect to FIG. 3C. Then, as was discussed with respect to FIGs. 3D through 3F, the silicon oxide layer 48 is first etched to form the trenches 50a through 50e. The trench etching is followed by patterning and etching of the via 52. A tantalum nitride liner 52 and copper are then deposited to form the wires or lines of metallization 56a through 56e followed by Chemical Mechanical Polishing of the copper to allow for still another layer of electronic elements and/or metallization. Thus, another difference in a structure manufactured according to the present invention compared to FIGs. 3F and 3G is that the lines of metallization are separated by the dummy fill dielectric structures 64a and 64b and therefore, there is little danger of a short between the metallization level 26.